WHAT IS CLAIMED IS:

1. Digital circuitry, operative repetitively to perform a series of processing cycles, comprising:

input signal processing means operable in each cycle to perform a predetermined processing operation on one or more input signals received by the circuitry to derive therefrom one or more first signals, said predetermined processing operation being commenced in response to a first clock signal;

first clocked means switchable, by application thereto of a second clock signal, between a responsive state, in which the first clocked means are operable in response to a change in the first signal(s) to change one or more second signals produced thereby, and a non-responsive state in which no change in the second signal(s) occurs;

second clocked means switchable, by application thereto of a third clock signal, between a responsive state, in which the second clocked means are operable in response to a change in the second signal(s) to change one or more output signals of the circuitry, and a non-responsive state in which no change in the output signal(s) occurs; and

clock generating means for deriving the second and third clock signals from the first clock signal, the second clock signal being delayed relative to the first clock signal by a preselected delay time and said third clock signal being delayed relative to the first clock signal by less than said preselected delay time such that in each cycle the first clocked means enter said non-responsive state before the end of said predetermined processing operation, and said second clocked means enter said responsive state when the first clocked means are in said non-responsive state.

2. Digital circuitry as claimed in claim 1, wherein said third clock signal has no or no

substantial delay relative to said first clock signal.

3. Digital circuitry as claimed in claim 1, wherein said preselected delay time is chosen such that said first clocked means enter said non-responsive state at least a predetermined hold time before the end of said predetermined processing operation, which predetermined hold time is the minimum period for which the or each first signal must remain stable after the first clocked means enter said non-responsive state.

4. Digital circuitry as claimed in claim 1, wherein said clock generating means are such that a predetermined enabling change in said third clock signal, which change causes the second clocked means to change from said non-responsive state to said responsive state, occurs substantially simultaneously with one of the changes in said first clock signal.

5. Digital circuitry as claimed in claim 4, wherein said one change in the first clock signal is a predetermined enabling change in that signal which causes said predetermined processing operation to commence.

6. Digital circuitry as claimed in claim 4, wherein a predetermined disabling change in the third clock signal, which change causes the second clocked means to change from said responsive state to said non-responsive state, is delayed substantially relative to one of the changes in the first clock signal.

7. Digital circuitry as claimed in claim 6, wherein the clock generating means include:

delay means for delaying the first clock signal to produce a delayed version thereof; and

logic means for logically combining the first clock signal with said delayed version thereof such that said enabling change in the third clock signal is substantially simultaneous with said enabling change in said first clock signal, and said disabling change in

the third clock signal is substantially simultaneous with one of the changes in said delayed version of the first clock signal.

8. Digital circuitry as claimed in claim 7, wherein said clock generating means further include delay balancing means connected between said delay means and said first clocked means for receiving said delayed version of the first clock signal and for deriving therefrom said second clock signal, the delay balancing means having a first propagation delay between said one change in the delayed version of the first clock signal and a predetermined enabling change in said second clock signal that causes the first clocked means to change from said non-responsive state to said responsive state, said first propagation delay being substantially equal to a second propagation delay, of said logic means, between said one change in said delayed version and said disabling change in the third clock signal.

9. Digital circuitry as claimed in claim 1, wherein said input signal processing means include further clocked means switchable, by application thereto of said first clock signal, between a responsive state, in which said further clocked means are operable in response to a change in said input signal(s) to change one or more basic signals produced thereby, and a non-responsive state in which no change in the basic signal(s) occurs; and

signal processing means for deriving said one or more first signals from the basic signal(s).

10. Digital circuitry as claimed in claim 1, wherein said first clocked means include a D-type latch element.

11. Digital circuitry as claimed in claim 1, wherein said second clocked means include a transparent half latch element.

12. Digital circuitry as claimed in claim 1, wherein said first signals and/or said second signals and/or said third signals and/or said output signals are complementary signal pairs.

13. Digital circuitry as claimed in claim 1, wherein the or each first signal and/or the or each second signal and/or the or each third signal and/or the or each output signal is a thermometer-coded signal.

14. Digital circuitry as claimed in claim 1, further including power supply means for supplying power to said second clocked means independently from that supplied to at least another part of said digital circuitry.

15. Digital circuitry as claimed in claim 1, including a plurality of individual circuit units, each circuit unit including such input signal processing means and such first clocked means and such second clocked means.

16. Digital circuitry as claimed in claim 15, wherein the clock generating means include:

a global clock generator provided in common for all said circuit units and operable to produce a basic clock signal; and

a plurality of local clock drivers, each corresponding to one or more of said circuit units, and each being connected to the global clock generator for receiving therefrom said basic clock signal and being operable to derive therefrom a unique such third clock signal for application to said second clocked means in the or each of its said one or more corresponding circuit units.

17. Digital circuitry as claimed in claim 16, wherein each said circuit unit has its own individually-corresponding one of said local clock drivers.

18. Digital circuitry as claimed in claim 16, wherein said global clock generator is operable to produce respective mutually-complementary such basic clock signals which are applied in common to all of said local clock drivers of said plurality.

19. Digital circuitry as claimed in claim 15, further comprising power supply decoupling means for decoupling from one another the respective power supplies of respective predetermined parts of at least two different circuit units of said plurality.

20. Digital circuitry as claimed in claim 19, wherein said power supply decoupling means are operable to decouple the power supply of such a predetermined part of each said circuit unit from that of each other one of the circuit units.

21. Digital circuitry as claimed in claim 19, wherein said predetermined part of said circuit unit includes said second clocked means.

22. Digital circuitry as claimed in claim 17, further comprising power supply decoupling means for decoupling from one another the respective power supplies of respective predetermined parts of at least two different circuit units of said plurality;

wherein said predetermined part of said circuit unit includes said second clocked means and said local clock driver of the circuit unit.

23. Mixed-signal circuitry including:

digital circuitry, operative repetitively to perform a series of processing cycles, comprising:

input signal processing means operable in each cycle to perform a predetermined processing operation on one or more input signals received by the circuitry to derive therefrom one or more first signals, said predetermined processing operation being commenced in response to a first clock signal;

first clocked means switchable, by

application thereto of a second clock signal, between a responsive state, in which the first clocked means are operable in response to a change in the first signal(s) to change one or more second signals produced thereby, and a non-responsive state in which no change in the second signal(s) occurs;

second clocked means switchable, by application thereto of a third clock signal, between a responsive state, in which the second clocked means are operable in response to a change in the second signal(s) to change one or more output signals of the circuitry, and a non-responsive state in which no change in the output signal(s) occurs; and

clock generating means for deriving the second and third clock signals from the first clock signal, the second clock signal being delayed relative to the first clock signal by a preselected delay time and said third clock signal being delayed relative to the first clock signal by less than said preselected delay time such that in each cycle the first clocked means enter said non-responsive state before the end of said predetermined processing operation, and said second clocked means enter said responsive state when the first clocked means are in said non-responsive state; and

analog circuitry connected to said digital circuitry for receiving therefrom said one or more output signals and operable to produce one or more analog signals in dependence upon the received output signal(s).

24. Mixed-signal circuitry as claimed in claim 23, including a digital-to-analog converter.

25. Mixed-signal circuitry as claimed in claim 23, wherein the analog circuitry includes a plurality of current sources or current sinks and a plurality of switch circuits connected to the current sources/sinks

for performing predetermined switching operations in dependence upon said output signal(s) so as to produce said one or more analog signals.

26. Mixed-signal circuitry as claimed in claim 23, wherein said digital circuitry further includes power supply means for supplying power to the second clocked means independently from that supplied to at least another part of said digital circuitry; and

wherein said power supply means are also operable to supply power to said analog circuitry independently of the power supplied to the or each said second clocked means and to said other part of the digital circuitry.

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